LISTING OF THE CLAIMS:

Claim 1 (Currently Amended) A method of fabricating a strained semiconductor-on-insulator (SSOI) comprising the steps of:

forming a second crystalline semiconductor layer that is strained on a surface of a first crystalline semiconductor layer, said first crystalline semiconductor layer is located atop an insulating layer of a preformed silicon-on-insulator (SOI) substrate, said insulating layer is a crystalline or non-crystalline oxide or nitride that is highly resistant to Ge diffusion;

subjecting the preformed SOI substrate containing the second crystalline semiconductor layer to a first annealing step at a first temperature that is sufficient to relax the strain in the second crystalline semiconductor layer;

performing an amorphization ion implantation to create a buried amorphized region comprising the entirety of the first crystalline semiconductor layer and a lower portion of the second crystalline semiconductor layer;

subjecting the preformed SOI substrate containing the second crystalline semiconductor layer and the buried amorphized region to a second annealing step at a second temperature sufficient to recrystallize the buried amorphized region resulting in said first crystalline semiconductor layer recrystallizing in a strained state; and

selectively removing the second crystalline semiconductor layer providing a strained semiconductor-on-insulator substrate.

Claim 2 (Cancelled)

Claim 3 (Original) The method of Claim 1 wherein the first crystalline semiconductor layer has thickness from about 5 to about 50 nm.

Claim 4 (Original) The method of Claim 1 wherein the first crystalline semiconductor layer comprises Si, SiC, SiGe, SiGeC, Ge, GaAs, InAs, InP, another III/V or II/VI compound semiconductor.

Claim 5 (Original) The method of Claim 4 wherein the first crystalline semiconductor layer is a Si-containing semiconductor.

Claim 6 (Original) The method of Claim 1 wherein the second crystalline semiconductor layer comprises Si, SiC, SiGe, SiGeC, Ge, GaAs, InAs, InP, another III/V or II/VI compound semiconductor.

Claim 7 (Original) The method of Claim 6 wherein the second crystalline semiconductor layer is a Ge-containing material.

Claim 8 (Original) The method of Claim 7 wherein the Ge-containing material is a SiGe alloy or pure Ge.

Claim 9 (Original) The method of Claim 1 wherein forming the second crystalline semiconductor layer comprises an epitaxial growth process.

Claim 10 (Original) The method of Claim 9 wherein the epitaxial growth process is selected from rapid thermal chemical vapor deposition, low-pressure chemical vapor deposition, ultra-high vacuum chemical vapor deposition, atmospheric pressure chemical vapor deposition, molecular beam epitaxy and plasma-enhanced chemical vapor deposition.

Claim 11 (Original) The method of Claim 1 wherein the second crystalline semiconductor layer has a thickness from about 10 to about 500 nm.

Claim 12 (Original) The method of Claim 1 further comprising performing a defect creating ion implantation to create defects within or near the first crystalline semiconductor layer between said forming and first annealing step.

Claim 13 (Original) The method of Claim 12 wherein the defect creating ion implantation is carried out using ions of hydrogen, deuterium, helium, oxygen, neon, boron, silicon or mixtures and isotopes thereof.

Claim 14 (Original) The method of Claim 13 wherein the ions are hydrogen or oxygen ions.

Claim 15 (Original) The method of Claim 12 wherein the defect creating ion implantation is carried out using an ion concentration of below 3E16 cm^{-2}.

Claim 16 (Currently Amended) The method of Claim 12 wherein the defects ~~can~~ serve as efficient ~~disclocation~~ dislocation nucleation sites which allow the second crystalline semiconductor layer to relax more efficiently.

Claim 17 (Original) The method of Claim 12 wherein the defect creating ion implantation is performed using an implantation mask.

Claim 18 (Original) The method of Claim 1 wherein the first annealing step is performed in an inert gas ambient or a forming gas ambient.

Claim 19 (Original) The method of Claim 1 wherein the first temperature of the first annealing step is from about 700°C to about 1100°C.

Claim 20 (Original) The method of Claim 1 wherein the first annealing step is carried out using a rapid thermal annealing process, a furnace annealing process, a laser annealing process of a spike anneal.

Claim 21 (Original) The method of Claim 1 wherein the amorphization ion implantation is carried out using ions selected from Si, P, As, Ge, C and any combination thereof.

Claim 22 (Original) The method of Claim 1 wherein the second annealing step is performed in an inert gas ambient or a forming gas ambient.

Claim 23 (Original) The method of Claim 1 wherein the second temperature of the second annealing step is from about 600°C to about 1100°C.

Claim 24 (Original) The method of Claim 1 wherein the second annealing step is carried out using a rapid thermal annealing process, a furnace annealing process, a laser annealing process of a spike anneal.

Claim 25 (Original) The method of Claim 1 wherein the selectively removing comprises chemical etching, reactive ion etching, low-temperature oxidation, atomic oxidation, chemical mechanical polishing, gas-cluster beam thinning or any combination thereof.

Claim 26 (Currently Amended) A method of fabricating a strained semiconductor-on-insulator (SSOI) comprising the steps of:

forming a second crystalline semiconductor layer that is strained on a surface of a first crystalline semiconductor layer, said first crystalline semiconductor layer is located atop an insulating layer of a preformed silicon-on-insulator (SOI) substrate, <u>said insulating layer is a crystalline or non-crystalline oxide or nitride that is highly resistant to Ge diffusion;</u>

performing a defect creating ion implantation to create defects within or near the first crystalline semiconductor layer;

subjecting the preformed SOI substrate containing the second crystalline semiconductor layer and the defects to a first annealing step at a first temperature that is sufficient to relax the strain in the second crystalline semiconductor layer;
performing an amorphization ion implantation to create a buried amorphized region comprising the entirety of the first crystalline semiconductor layer and a lower portion of the second crystalline semiconductor layer;

subjecting the preformed SOI substrate containing the second crystalline semiconductor layer and the buried amorphized region to a second annealing step at a second temperature sufficient to recrystallize the buried amorphized region resulting in said first crystalline semiconductor layer recrystallizing in a strained state; and

selectively removing the second crystalline semiconductor layer providing a strained semiconductor-on-insulator substrate.

Claim 27 (Cancelled)

Claim 28 (Original) The method of Claim 26 wherein the first crystalline semiconductor layer has thickness from about 5 to about 50 nm.

Claim 29 (Original) The method of Claim 26 wherein the first crystalline semiconductor layer comprises Si, SiC, SiGe, SiGeC, Ge, GaAs, InAs, InP, another III/V or II/VI compound semiconductor.

Claim 30 (Original) The method of Claim 29 wherein the first crystalline semiconductor layer is a Si-containing semiconductor.

Claim 31 (Original) The method of Claim 26 wherein the second crystalline semiconductor layer comprises Si, SiC, SiGe, SiGeC, Ge, GaAs, InAs, InP, another III/V or II/VI compound semiconductor.

Claim 32 (Original) The method of Claim 31 wherein the second crystalline semiconductor layer is a Ge-containing material.

Claim 33 (Original) The method of Claim 32 wherein the Ge-containing material is a SiGe alloy or pure Ge.

Claim 34 (Original) The method of Claim 26 wherein forming the second crystalline semiconductor layer comprises an epitaxial growth process.

Claim 35 (Original) The method of Claim 34 wherein the epitaxial growth process is selected from rapid thermal chemical vapor deposition, low-pressure chemical vapor deposition, ultra-high vacuum chemical vapor deposition, atmospheric pressure chemical vapor deposition, molecular beam epitaxy and plasma-enhanced chemical vapor deposition.

Claim 36 (Original) The method of Claim 26 wherein the second crystalline semiconductor layer has a thickness from about 10 to about 500 nm.

Claim 37 (Original) The method of Claim 26 wherein the defect creating ion implantation is carried out using ions of hydrogen, deuterium, helium, oxygen, neon, boron, silicon or mixtures and isotopes thereof.

Claim 38 (Original) The method of Claim 37 wherein the ions are hydrogen or oxygen ions.

Claim 39 (Original) The method of Claim 26 wherein the defect creating ion implantation is carried out using an ion concentration of below 3E16 cm^{-2}.

Claim 40 (Currently Amended) The method of Claim 26 wherein the defects ~~can~~ serve as efficient dislocation nucleation sites which allow the second crystalline semiconductor layer to relax more efficiently.

Claim 41 (Original) The method of Claim 26 wherein the defect creating ion implantation is performed using an implantation mask.

Claim 42 (Original) The method of Claim 26 wherein the first annealing step is performed in an inert gas ambient or a forming gas ambient.

Claim 43 (Original) The method of Claim 26 wherein the first temperature of the first annealing step is from about 700°C to about 1100°C.

Claim 44 (Original) The method of Claim 26 wherein the first annealing step is carried out using a rapid thermal annealing process, a furnace annealing process, a laser annealing process or a spike anneal.

Claim 45 (Original) The method of Claim 26 wherein the amorphization ion implantation is carried out using ions selected from Si, P, As, Ge, C and any combination thereof.

Claim 46 (Original) The method of Claim 26 wherein the second annealing step is performed in an inert gas ambient or a forming gas ambient.

Claim 47 (Original) The method of Claim 26 wherein the second temperature of the second annealing step is from about 600°C to about 1100°C.

Claim 48 (Original) The method of Claim 26 wherein the second annealing step is carried out using a rapid thermal annealing process, a furnace annealing process, a laser annealing process or a spike anneal.

Claim 49 (Original) The method of Claim 26 wherein the selectively removing comprises chemical etching, reactive ion etching, low-temperature oxidation, atomic

oxidation, chemical mechanical polishing, gas-cluster beam thinning or any combination thereof.

Claim 50 (Currently Amended) A method of fabricating a strained Si-on-insulator (SSOI) comprising the steps of:

forming a Ge-containing layer that is strained on a surface of a Si-containing layer, said Si-containing layer is located atop an insulating layer of a preformed silicon-on-insulator (SOI) substrate, said insulating layer is a crystalline or non-crystalline oxide or nitride that is highly resistant to Ge diffusion;

subjecting the preformed SOI substrate containing the Ge-containing to a first annealing step at a first temperature that is sufficient to relax the strain in the Ge-containing layer;

performing an amorphization ion implantation to create a buried amorphized region comprising the entirety of the Si-containing layer and a lower portion of the Ge-containing layer;

subjecting the preformed SOI substrate containing the Ge-containing layer and the buried amorphized region to a second annealing step at a second temperature sufficient to recrystallize the buried amorphized region resulting in said Si-containing layer recrystallizing in a strained state; and

selectively removing the Ge-containing layer providing a strained Si-containing-on-insulator substrate.

Claim 51 (Original) The method of Claim 50 wherein the insulating layer is a crystalline or non-crystalline oxide or nitride that is highly resistant to Ge diffusion.

Claim 52 (Original) The method of Claim 50 wherein the Si-containing layer has thickness from about 5 to about 50 nm.

Claim 53 (Original) The method of Claim 50 wherein the Ge-containing layer is a SiGe alloy or pure Ge.

Claim 54 (Original) The method of Claim 50 wherein the forming the Ge-containing layer comprises an epitaxial growth process selected from rapid thermal chemical vapor deposition, low-pressure chemical vapor deposition, ultra-high vacuum chemical vapor deposition, atmospheric pressure chemical vapor deposition, molecular beam epitaxy and plasma-enhanced chemical vapor deposition.

Claim 55 (Original) The method of Claim 50 wherein the Ge-containing layer has a thickness from about 10 to about 500 nm.

Claim 56 (Original) The method of Claim 50 further comprising performing a defect creating ion implantation to create defects within or near the first crystalline semiconductor layer between said forming and first annealing step.

Claim 57 (Original) The method of Claim 56 wherein the defect creating ion implantation is carried out using ions of hydrogen, deuterium, helium, oxygen, neon, boron, silicon or mixtures and isotopes thereof.

Claim 58 (Original) The method of Claim 57 wherein the ions are hydrogen or oxygen ions.

Claim 59 (Original) The method of Claim 57 wherein the defect creating ion implantation is carried out using an ion concentration of below 3E16 cm^{-2}.

Claim 60 (Currently Amended) The method of Claim 57 wherein the defects ~~can~~ serve as efficient dislocation nucleation sites which allow the second crystalline semiconductor layer to relax more efficiently.

Claim 61 (Original) The method of Claim 57 wherein the defect creating ion implantation is performed using an implantation mask.

Claim 62 (Original) The method of Claim 50 wherein the first annealing step is performed in an inert gas ambient or a forming gas ambient.

Claim 63 (Original) The method of Claim 50 wherein the first temperature of the first annealing step is from about 700°C to about 1100°C.

Claim 64 (Original) The method of Claim 50 wherein the first annealing step is carried out using a rapid thermal annealing process, a furnace annealing process, a laser annealing process or a spike anneal.

Claim 65 (Original) The method of Claim 50 wherein the amorphization ion implantation is carried out using ions selected from Si, P, As, Ge, C and any combination thereof.

Claim 66 (Original) The method of Claim 50 wherein the second annealing step is performed in an inert gas ambient or a forming gas ambient.

Claim 67 (Original) The method of Claim 50 wherein the second temperature of the second annealing step is from about 600°C to about 1100°C.

Claim 68 (Original) The method of Claim 50 wherein the second annealing step is carried out using a rapid thermal annealing process, a furnace annealing process, a laser annealing process or a spike anneal.

Claim 69 (Original) The method of Claim 50 wherein the selectively removing comprises chemical etching, reactive ion etching, low-temperature oxidation, atomic

oxidation, chemical mechanical polishing, gas-cluster beam thinning or any combination thereof.